



## DESCRIPTION

The A7512 is a monolithic step-down DC to DC converter. The A7512 works from a 4.75V to 20V input voltage range, and offers up to 2A of continuous output current in a compact SOP8 package.

The A7512 operates in voltage mode. Lower quiescent current and wider operating input-voltage range are implemented by high-voltage BICMOS-based technology. Alternative PWM/PFM control technique significantly improves the efficiency for both light load and heavy load.

The A7512 also integrates soft-start, over load protection and under voltage lockout protection etc., which minimized external components and converter size.

The A7512 is available in SOP8 & P-SOP8 package.

## ORDERING INFORMATION

Package Type	Part Number	
SOP8	M	A7512M8R
P-SOP8	MP	A7512MP8R
Note	R : Tape & Reel	
AiT provides all Pb free products		

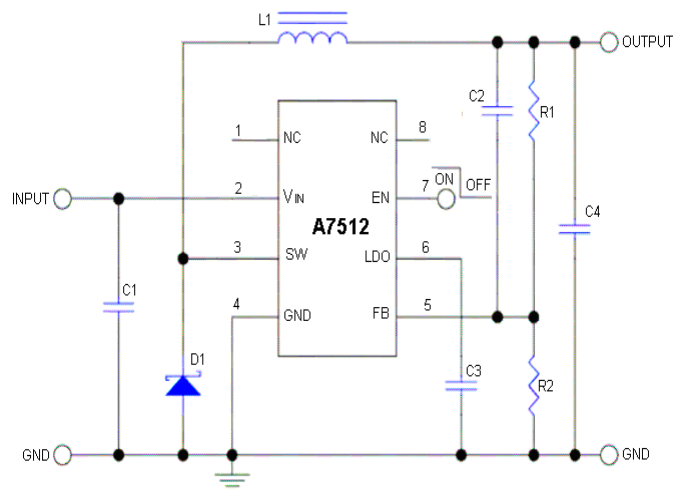
## FEATURES

- Built-in 90mΩ P-Channel MOSFET
- Wide 4.75~20V input Voltage Range
- Adaptive PWM/PFM Operation Mode
- Up to 95% Efficiency
- Built-in Soft-Start Function
- Fault Protection (Auto Recovery Mode)
- <1 μA Shutdown Current and 350 μA Quiescent Current
- Low Temperature-Drift Coefficient of Bandgap Voltage
- Available in SOP8 & P-SOP8 Package

## APPLICATION

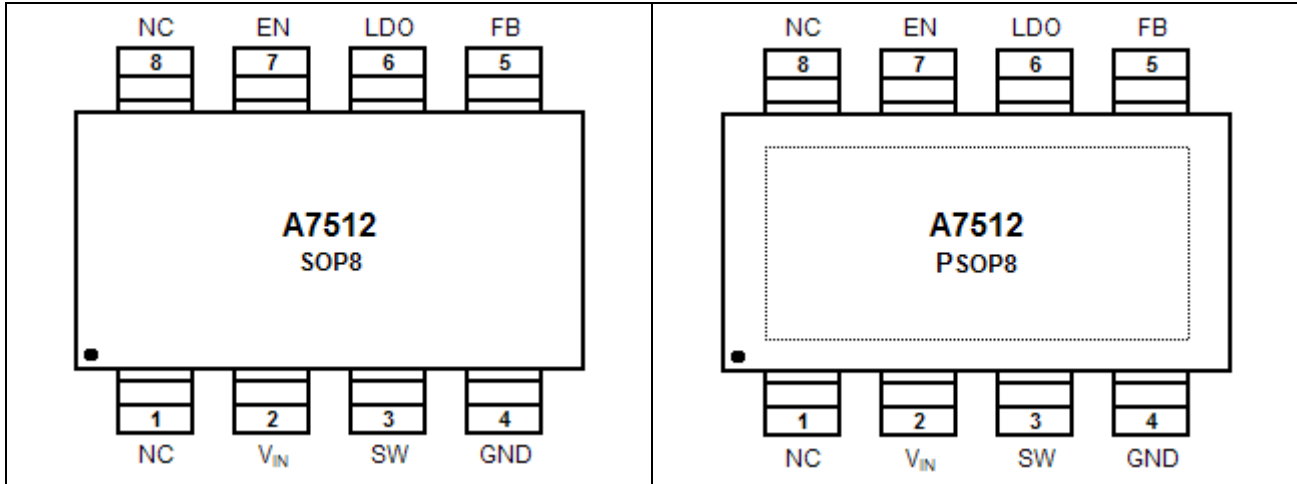
- Power Source for Battery-Powered Equipments.
- Distribute DC to DC Power Supply
- Pre-Regulator for Linear Regulator

## TYPICAL APPLICATION





## PIN DESCRIPTION



Pin No.	Name	Function Description
1	NC	Not connected
2	V <sub>IN</sub>	Power supply input pin.
3	SW	Switching node. PWM output connection to inductor.
4	GND	Ground
5	FB	Feedback pin. It is used to program the output voltage by adjusting the ratio of the external resistor divider from output to ground. A compensation capacitor paralleling with the upper resistor is recommended to improve system dynamic response.
6	LDO	LDO output pin. A 0.1uF capacitor is recommended in order to filter the switching noise.
7	EN	Chip enable pin. High level activates the chip. Connect the pin to V <sub>IN</sub> if not used, do not leave the pin floating.
8	NC	Not connected



## ABSOLUTE MAXIMUM RATINGS

Supply Voltage: $V_{IN}$	-0.3~25V
Switch Node: SW	-0.3V~(Vin+0.3V)
Chip Enable: CE	-0.3V~(Vin+0.3V)
Feedback Input: FB	-0.3~6V
LDO Output: LDO	-0.3~6V
Junction Temperature	150 °C
Storage Temperature Range	-40~150 °C
Lead Temperature and Time	260 °C, 10s

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

ITEMS	MIN	NOM	MAX	UNIT
Input Voltage Range	4.75		20	V
Operating Temperature	125		85	°C

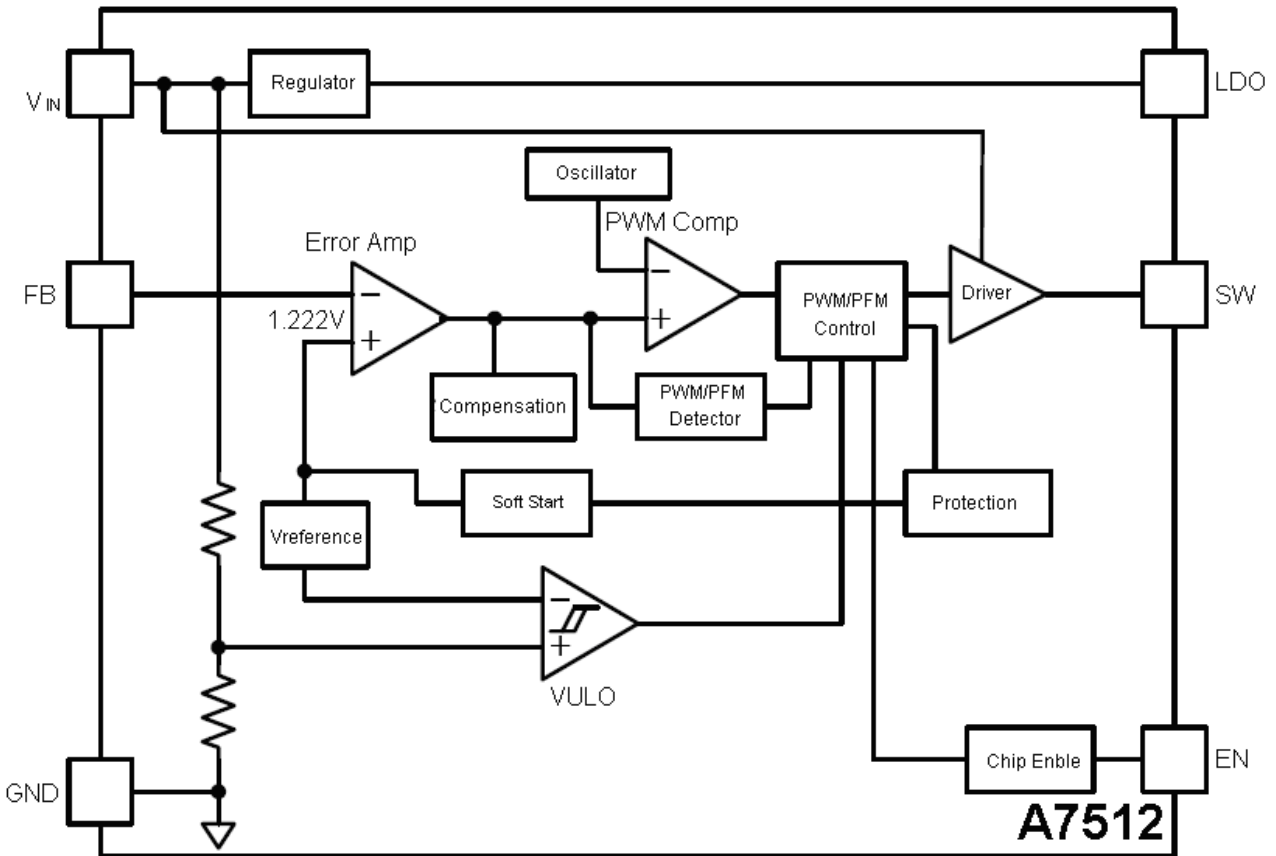
Note 1. Exceeding these ratings may damage the device

Note 2. Measured on approximately 1" square of 1 oz copper.

Note 3. The device is not guaranteed to function outside its operating rating



**BLOCK DIAGRAM**





## ELECTRICAL CHARACTERISTICS

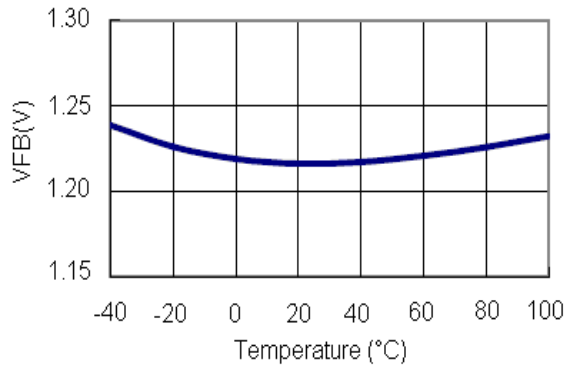
Unless otherwise specified,  $V_{IN}=12V$ ,  $C_{LDO}=0.1\mu F$ ,  $T_A=25^\circ C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Operation Input Voltage		4.75		20	V
$R_{DS(ON)}$	Static P-Channel MOSFET On State Resistance	$V_{CE}=12V$ ; $I_{FB}=0V$		90*		m $\Omega$
$V_{FB}$	Feedback Voltage	$V_{CE}=12V$ ; $L_{OUT}=-100mA$	1.198	1.222	1.246	V
$F_{OSC}$	Oscillator Frequency	$V_{CE}=12V$ ; $L_{OUT}=-100mA$	550	550	600	KHz
$I_{DD}$	Quiescent Current (Operating)	$V_{CE}=12V$ ; $V_{FB}=1.4V$			350	$\mu A$
$I_{SD}$	Shutdown Current	$V_{CE}=0V$			1	$\mu A$
$V_{CEH}$	CE "H" Threshold Voltage		1.5			V
$V_{CEL}$	CE "L" Threshold Voltage				0.7	V
$I_{CEH}$	CE "H" Input Current				0.3	$\mu A$
$I_{CEL}$	CE "L" Input Current		-0.3			$\mu A$
$V_{UVLO1}$	UVLO Threshold Voltage	$V_{IN} = V_{CE} = 5$ to $0V$	1.5	1.9	2.3	V
$V_{UVLO2}$	UVLO Release Voltage	$V_{IN} = V_{CE} = 0$ to $5V$	1.6	2.0	2.4	V
$MAX_{DTY}$	Max. Duty Cycle		100			%
$T_{START}$	Soft-Start Time	$V_{CE} = 0$ to $12V$	5	10	15	ms
$T_{PRO}$	Debounce Time for Fault Protection	$V_{CE}=12V$ ; $V_{FB}=0$	500	700	1000	$\mu s$
$LDO$	LDO Output Voltage	$V_{IN} > 6V$ ; $V_{CE} = V_{IN}$		5		V

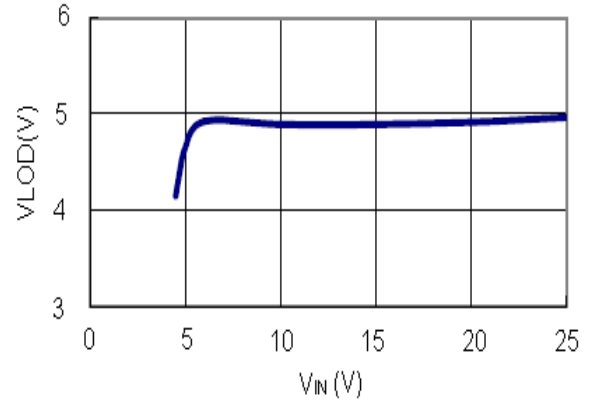


## TYPICAL PERFORMANCE CHARACTERISTICS

1. Reference Voltage vs. Temperature

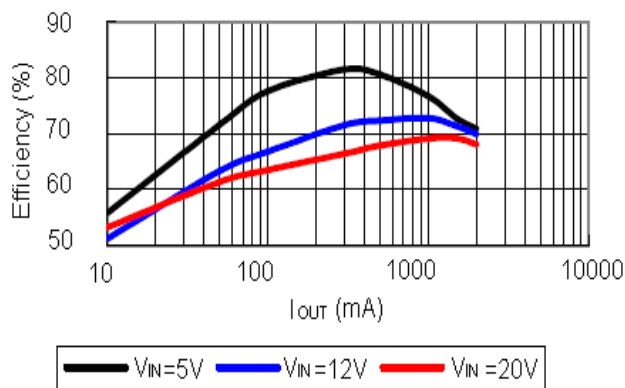


2. LDO Regulation vs. Input Voltage



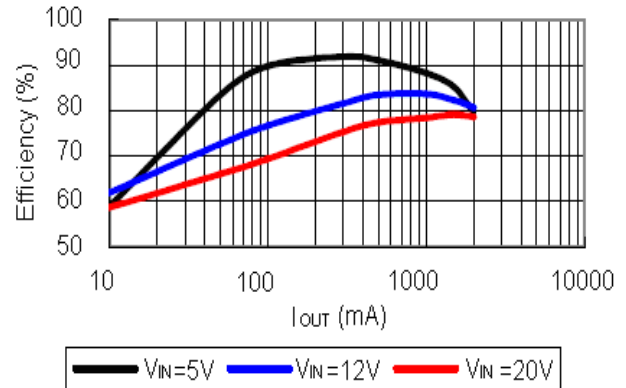
3. Efficiency vs. Output Current

V<sub>OUT</sub>=1.8V



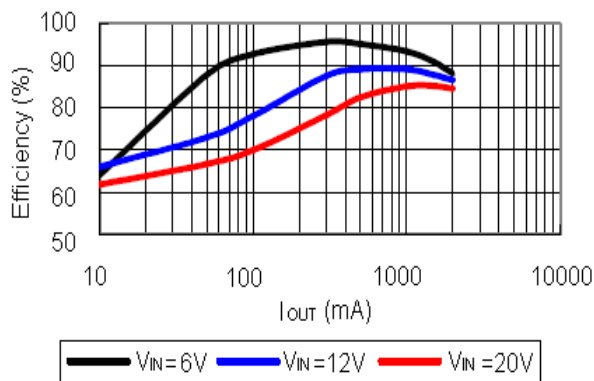
4. Efficiency vs. Output Current

V<sub>OUT</sub>=3.3V



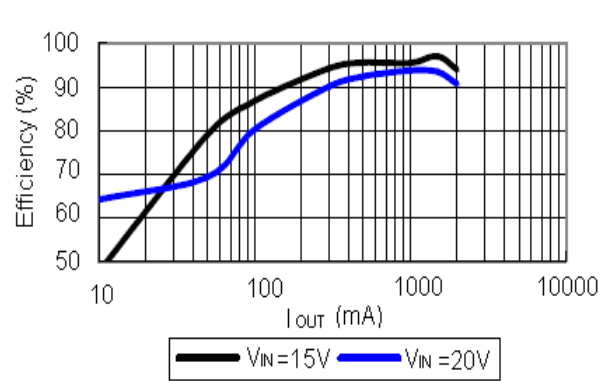
5. Efficiency vs. Output Current

V<sub>OUT</sub>=5V



6. Efficiency vs. Output Current

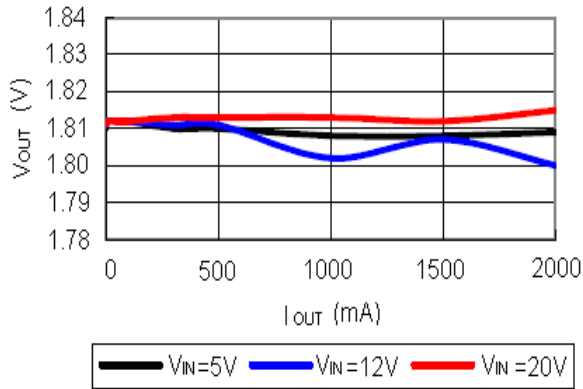
V<sub>OUT</sub>=12.3V





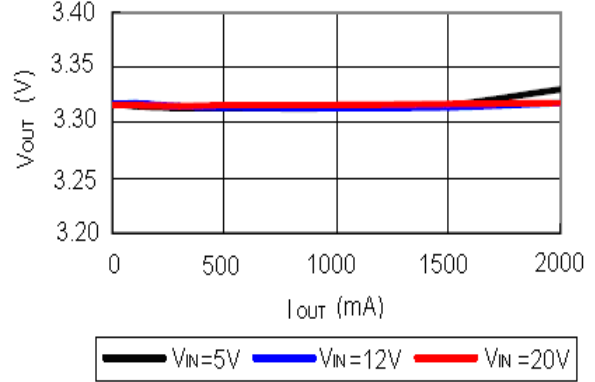
7.Regulation vs. Output Current

$V_{OUT}=1.8V$



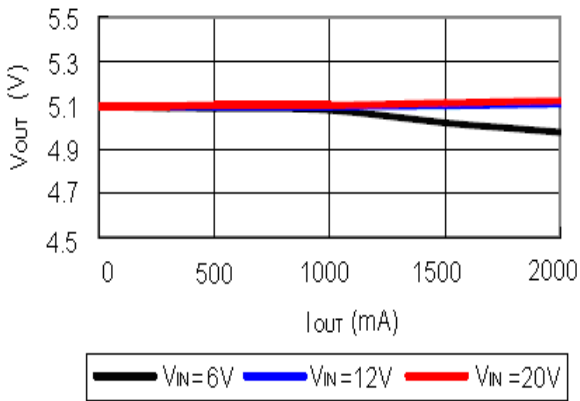
8.Regulations vs. Output Current

$V_{OUT}=3.3V$



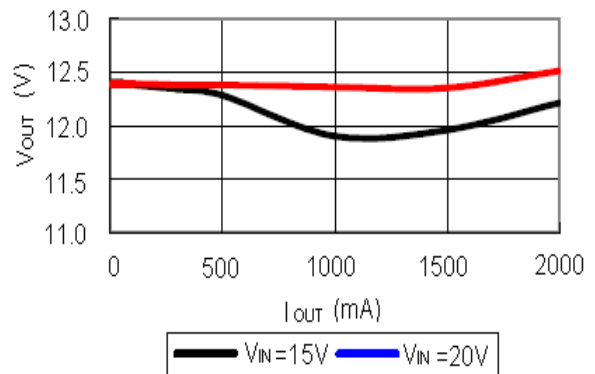
9.Regulations vs. output current

$V_{OUT}=5V$



10.Regulations vs. Output Current

$V_{OUT}=12.3V$





## **DETAILED INFORMATION**

A7512 consists of a P-channel MOSFET, an oscillator, a PWM control circuit, a voltage reference unit, an error amplifier, a soft-start circuit, a fault protection circuit, a PWM/PFM alternative circuit, a chip enable circuit, and an input voltage detecting circuit.

### **PWM Operation**

In normal operation, adjusting the width of pulse regulates the system output voltage. It is implemented by regulating the FB voltage at 1.222V. The A7512 high-gain differential error amplifier and low temperature-drift coefficient reference guarantee the accuracy of output voltage with different input voltage and load conditions. In order to reduce the ripple voltage and improve the loop stability, a high bandwidth error amplifier is designed with a built-in zero. This zero, plus the ESR zero from the output electrolytic capacitor, balances the double poles of the output LC filter. Thus the step-down system is stable and external compensation network is not required. In practice, a low cost ceramic capacitor paralleling with the upper resistor on feedback resistors divider implements additional phase lead compensation function. This improves the dynamic response performance. In order to improve the efficiency, The A7512 integrates a low on-resistance P-channel MOSFET and well designed driver circuits inside a SOP8 package, the power loss is limited at very low level.

### **PFM Operation**

At light load, the error amplifier's output voltage becomes very low and the duty cycle becomes very small. The system switching losses dominate and conduction losses become less important. The A7512 limits its minimum duty cycle. If the output current is low enough, the output voltage exceeds the desired value and the error amplifier output voltage decreases down to 0.6V, then the output pulse are disabled and the system output voltage decreases until the error amplifier output ramps up above the threshold of 0.6V. Thus the switching node waveform looks like a pulse-skipping mode. The number of pulses and switching losses are significantly reduced.

### **Oscillator**

The oscillator circuit provides a clock to set the converter operating frequency.

### **Protection Circuit**

If the duration of maximum duty cycle is long enough, the embedded protection circuit shuts down internal power switch. Then the IC starts a soft start cycle. This procedure repeats until the cause of the protection condition is removed.



### **Soft-Start**

A small current charges the soft-start capacitor and raises the internal soft start voltage. The reference voltage follows the soft-start voltage, and limits the speed of voltage rising on the error amplifier output, and hence reduces the speed of rising of output voltage during startup.

### **UVLO**

If the input voltage is equal or less than UVLO threshold, the IC goes to standby mode. If the input voltage increases above the UVLO threshold with a hysteresis voltage, the IC starts another soft-start cycle and normal operation.

### **Enable (CE)**

Logic low on CE puts the A7512 in shutdown state. In shutdown mode, the output power switch, voltage reference, and other functions are shut off, the supply current is reduced to 1  $\mu$ A maximum.

## **NOTIFICATION**

Be aware of the following issues while using the A7512:

Set external components as close as possible to the IC and minimize the connection between the components and the IC. In particular, the power rails and SW connection should be short. In addition, a ceramic capacitor should be closely connected between LDO and GND pins. Make sufficient grounding and reinforce supplying.

If the difference between input and output voltage is too small, the maximum duty cycle may last long enough to trigger the maximum duty-cycle protection.

If input voltage is below 6V, the LDO output may drop below 5V, and the maximum duty cycle may be limited. The accuracy of load regulation may be limited by current capability if output voltage gets close to input voltage.

If the duty cycle in PWM mode needs to be less than the minimum duty cycle to go to PFM mode, the IC switches to PFM mode to reduce switching frequency and standby current. However, if the ratio of output voltage vs. input voltage is low enough (for example,  $V_{IN}>12V$  and  $V_{OUT}=1.5V$ ), even if the load current is large, the IC keeps in PFM mode, and the ripple of output voltage may increase.



## COMPONENTS SELECTION

### Inductor

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, and hence reduces conduction loss. Usually, peak to peak current of inductor is designed to be 20% to 30% of output current.

### Diode

Use a diode with low forward voltage drop and high switching speed. (Schottky type is recommended.)

Reverse voltage rating should be more than the input voltage, and current rating should be more than maximum load current.

### Capacitors

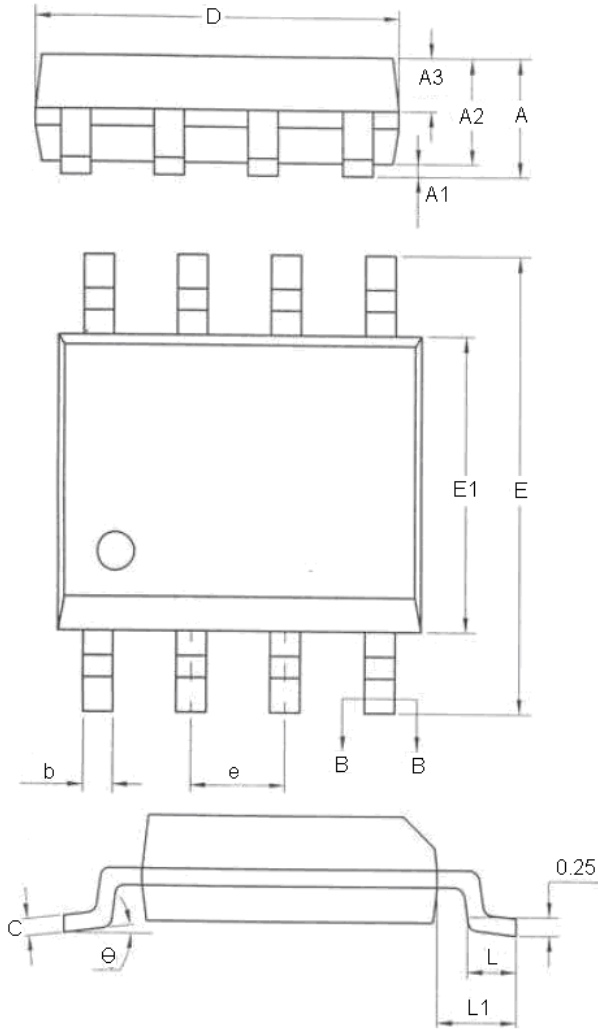
The primary function of output capacitor is to smooth the inductor current. The actual output ripple voltage is a function of this capacitor's ESR (Equivalent Series Resistance). Normally the ESR of this capacitor should not exceed the rated ripple voltage divided by the ripple current through the inductor.

As for input capacitor, use a capacitor with low ESR and a capacity of at least  $\mu\text{F}$  for stable operation.

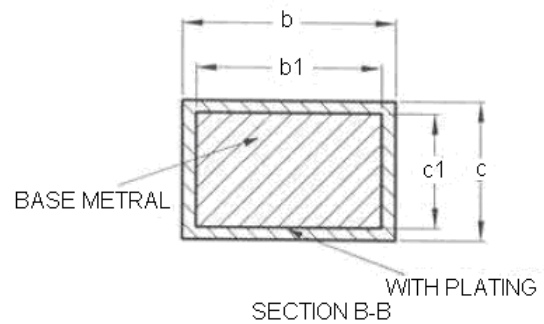


**PACKAGE INFORMATION**

Dimension in SOP8 Package (Unit: mm)



SYMBOL	MIN	NOM	MAX
A	—	—	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	—	0.48
b1	0.38	0.41	0.43
C	0.21	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
	0	—	





## **IMPORTANT NOTICE**

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